CPRE 4910 Weekly Report 06

10/27/2025 - 11/3/2025

Group number: SDMay26-24

Project title: Digital ASIC Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:

Colin McGann	***-Project Lead***
Samuel Forde	***-PCB & Layout Lead***
Michael Drobot	***-Firmware Lead***
Jack Tonn	***-Testbench and Validation Lead***
Dawud Benedict	***-Toolflow Lead***
Emil Kosic	***-Repository and Coding Standards Lead***
Joshua Arceo	***-Client/Advisor Communications Lead***

- **Weekly Summary**

This week we continued to integrate the VGA and SPI-mem modules to get output on a monitor. The ISA/Core group worked to further define the desired properties of the cores and to create a model of the cores.

- **Past Week Accomplishments**
    - Colin McGann: Worked on getting the SPI memory system to work and fixed undefined behavior in our top level FPGA project
    - Jack Tonn: Defined preliminary core design and list of basic operations that we may want to use with our cores.
    - Dawud Benedict: Continued working on WB-PK bridge. Stayed in contacted with the Analog team for Cadence tool integration.
    - Michael Drobot: Started top-level-design testing and firmware, wrote 3D model vertex shading script to use with the rasterizer testbench, and helped integration test the SPI memory controller and VGA on FPGA.

- Sam Forde: Helped write the design portion of the design document. Got a single mac unit into Caravel harness, started on testing and working on integrating other designs.
- Josh Arceo: Created a few more sample fragment shaders, and a way to test fragment shading by by changing light source position
- Emil Kosic: Learned behavioral Verilog. Designed global and local registers for GPU cores.

- **Pending Issues**
  - Get the SPI memory controller, PKBus, and VGA to work on the FPGA. The issues we found so far have been in the memory controller, in the PKBus stream protocol, the ChipForge FPGA tooling, and in Vivado's FPGA synthesis.
  - Table of ISA instructions, operands, and algorithms the instructions would be used in.
  - Predication implementation in the cores

- **Individual contributions**

NAME	Individual Contributions	Hours this week	HOURS cumulative
Colin McGann	FPGA and SPI memory controller work	20	100
Jack Tonn	Core model and ISA operations	7	41
Dawud Benedict	WB-PK bridge, Cadence tools	6	38
Michael Drobot	Top-level firmware, 3D model conversion script	15	65
Sam Forde	Design Doc, Integrating mac unit into Caravel	8	40
Josh Arceo	More fragment shaders, fragment shader verification tool	4	28
Emil Kosic	Core global and local registers	6	32

- **Plans for the upcoming week**
  - Colin McGann: Will continue working on our FPGA design and hook up the rasterizer to real hardware.
  - Jack Tonn: Define core instruction list and predication method. Delegate core work to other members of Core/ISA group.
  - Dawud Benedict: Complete PK-bridge, start memory hierarchy for cores.

    - Michael Drobot: Complete 3D model converter, continue integration testing SPI memory and VGA on FPGA, and start working on the core controller.
    - Sam Forde: Find a different part of the project to specialize into.
    - Josh Arceo: Work on Cache and memory hierarchy with Dawud
    - Emil Kosic: Continue designing GPU core components

- **<u>Advisor Meeting Summary</u>**